```
/* Initialise Zilog */
void init(void)
{
  int brg;
  const int bps = 57000;
  brg = BPS_TO_BRG(bps, ZS_CLOCK, 16);

  /* Reset */
  write_zsreg(R9, CHRA | NV);
  zs_udelay(10);

  /* Select no parity, 1 stop bit, 16xClock */
  write_zsreg(R4, SB1 | X16CLK);

  /* Rx 8 bits/char */
  write_zsreg(R3, Rx8);

  /* No interrupt */
  write_zsreg(R9, NV);

  /* Select NRZ, no loop stuff */
  write_zsreg(R10, NRZ);

  /* Select clock mode (no external sources) */
  write_zsreg(R11, TCBR | RCBR);

  /* Set BRG */
  write_zsreg(R12, (brg & 255));
  write_zsreg(R13, (brg >> 8) & 255);

  /* DTR follows DTR-bit in WR5 */
  write_zsreg(R14, BRSRC);
  write_zsreg(R14, BRSRC | BRENAB);

  /* Enable Rx */
  write_zsreg(R3, RxENAB | Rx8);

 /* Enable Tx (Note that DTR- and RTS-bits are low-active)*/
  write_zsreg(R5, TxENAB | Tx8 | RTS | DTR);

  /* No interrupts enabled */
  write_zsreg(R15, NOINTERRUPT);
  fprintf(stderr,
      "Waiting a moment until opposite ready ...\n");
  sleep(5);
}
```