

WRMSR—Write to Model Specific Register

Opcode	Instruction	Description
0F 30	WRMSR	Write the value in EDX:EAX to MSR specified by ECX

Description

Writes the contents of registers EDX:EAX into the 64-bit model specific register (MSR) specified in the ECX register. The high-order 32 bits are copied from EDX and the low-order 32 bits are copied from EAX. Always set the undefined or reserved bits in an MSR to the values previously read.

This instruction must be executed at privilege level 0 or in real-address mode; otherwise, a general protection exception #GP(0) will be generated. Specifying a reserved or unimplemented MSR address in ECX will also cause a general protection exception.

When the WRMSR instruction is used to write to an MTRR, the TLBs are invalidated, including the global entries (see “Translation Lookaside Buffers (TLBs)” in Chapter 3 of the *Intel Architecture Software Developer’s Manual, Volume 3*). (MTRRs are an implementation-specific feature of the Pentium Pro processor.)

The MSRs control functions for testability, execution tracing, performance monitoring and machine check errors. Appendix B, *Model-Specific Registers (MSRs)*, in the *Intel Architecture Software Developer’s Manual, Volume 3*, lists all the MSRs that can be written to with this instruction and their addresses.

The WRMSR instruction is a serializing instruction (see “Serializing Instructions” in Chapter 7 of the *Intel Architecture Software Developer’s Manual, Volume 3*).

The CPUID instruction should be used to determine whether MSRs are supported (EDX[5]=1) before using this instruction.

Intel Architecture Compatibility

The MSRs and the ability to read them with the WRMSR instruction were introduced into the Intel Architecture with the Pentium processor. Execution of this instruction by an Intel Architecture processor earlier than the Pentium processor results in an invalid opcode exception #UD.

Operation

MSR[ECX] ← EDX:EAX;

Flags Affected

None.



WRMSR—Write to Model Specific Register (Continued)**Protected Mode Exceptions**

- #GP(0) If the current privilege level is not 0.
 If the value in ECX specifies a reserved or unimplemented MSR address.

Real-Address Mode Exceptions

- #GP If the value in ECX specifies a reserved or unimplemented MSR address.

Virtual-8086 Mode Exceptions

- #GP(0) The WRMSR instruction is not recognized in virtual-8086 mode.